Hexapods and other high precision parallel kinematics in (industrial automation and) Silicon Photonics

C. Sander[x], C. Rudolf[x], A. Bogner[x]

[x]Physik Instrumente (PI) GmbH & Co. KG, Germany

c.sander@pi.de; c.rudolf@pi.de; a.bogner@pi.de

Abstract

The fast rise of Silicon Photonics (SiP) presents many challenges. Silicon Photonics is a combination of two very important inventions of the 20th century. The semiconductor laser and silicon integrated circuit. It enables faster data transfer and less power consumption[1] compared to traditional electronics.[2] Silicon photonics is not the same as the CMOS process used to make chips. It has its own manufacturing requirements that differ from those used to make pure electronic chips. These processes do not just include the wafer processing to make the photonic circuits but also custom circuit testing equipment and device packaging.[3] Among other things, the testing and the packaging processes make demands on new mechantronic systems, alignment algorithms (e.g., first light detection), and software solutions (as shown in figure 1 and figure 2).

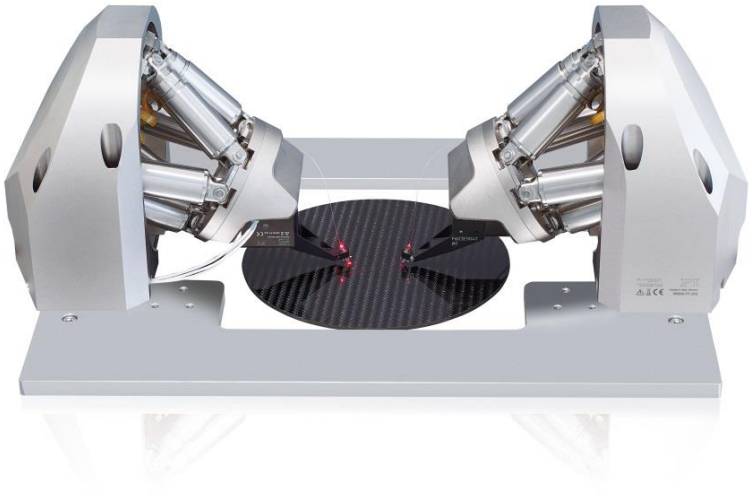

Figure 1: 18-axis double-sided fibre alignment system for silicon wafer testing

One of the key challenges is the need to align fiber optic devices to optimize optical throughput before testing and packaging can begin. In many cases, alignment in multiple degrees of freedom is required across more than one input and output coupling. Fast throughput is required in this highly accurate automated microprocess to increase the economic efficiency. To meet those needs, parallel-kinematic

[1] (Zhou et al. 2015)
[2] (Intel Corporation 2017)
[3] (Inniss & Rubenstein 2016)

systems with several degrees of freedom are used because of their high precision, stiffness, and speed. In addition to the stated advantages of parallel kinematics e.g., packaging processes using faser arrays benefit from the capability of defining any virtual pivot point to align multiple channels. A further increase of throughput can be realized by sophisticated controller algorithms . Within this contribution, different approaches and solutions for probing, chip and wafer testing, and packaging based on different technologies will be presented.

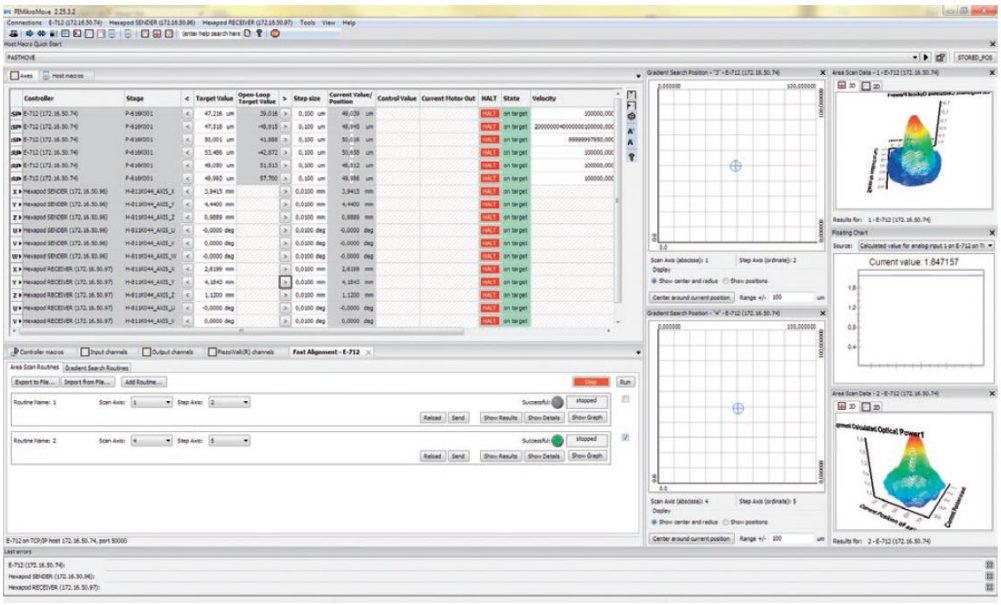

Figure 2: software solution for silicon wafer testing

Bibliography:

Inniss, D. & Rubenstein, R., 2016. *Silicon Photonics- Fueling the Next Information Revolution*, Morgan Kaufmann.

Intel Corporation, 2017. Intel® Silicon Photonics. Available at: https://www.intel.de/content/www/de/de/architecture-and-technology/silicon-photonics/silicon-photonics-overview.html [Accessed July 28, 2017].

Zhou, Z. et al., 2015. Lowering the energy consumption in silicon photonic devices and systems [Invited]. *Photonics Research*, 3(5), p.B28. Available at: http://dx.doi.org/10.1364/PRJ.3.000B28 [Accessed July 28, 2017].