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Sustainable manufacturing of metallic wires through solid-state processes with continuous Al6061 chips

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Abstract
As environmental challenges intensify and expectations for responsible manufacturing grow, sustainable process development is emerging as a strategic response. Solid-state processes provide a sustainable alternative to heat-based routes, reducing energy consumption and material waste. Prior work has explored the use of solid-state methods in transforming discontinuous machining chips into metallic wire in a melt-free manner. However, the discontinuous nature of the chips often introduces inter-chip interfaces and defects. Thus, this study proposes an alternative solid-state process that uses continuous Al6061 chips to produce wires. In this process, a controlled turning operation is conducted to generate long and continuous chips by varying cutting speed, uncut chip thickness, and tool cutting angles. Subsequently, the usability of the continuous chips was assessed through a tensile test. Variation of the three machining parameters produced either continuous smooth or serrated chips. The serration is a result of strain localization in the adiabatic shear band region, which is influenced by the three machining parameters through thermal softening. Tensile testing and fractography analysis indicated that non-serrated chips retain ductility and exhibit dimple dominated cup-and-cone fracture, whereas serrated chips show reduced load-carrying capacity associated with work hardening, and notch defects inherited from serration. As a result, serrated chips exhibited slant fracture, making them less ideal for subsequent deformation processing. As a preliminary feasibility assessment, this study validates the proposed solid-state process as a viable alternative method for producing thin metallic wires. Future studies will investigate the usability of the continuous wires produced through this method, particularly for wire-based additive manufacturing applications.

Sustainable manufacturing, machining chips, machining, finite element modelling

1. Introduction

As the manufacturing industry steers towards Industry 5.0, sustainable manufacturing processes have become the centre of focus in recent years. Sustainable manufacturing processes, such as the solid-state process, have gained attention as an innovative process to minimise emissions [1]. The solid-state process is often carried out under room temperature and pressure conditions, significantly reducing energy consumption. This is achieved through severe local plastic deformation, without the need for additional heat sources. The manufacturing of metallic wires, which are frequently used in additive manufacturing, automotive, and construction, is also an energy-intensive process. This is due to the repetitive wire drawing process at high temperature conditions to achieve the desired diameter. Subsequently, the wires undergo heat treatments such as annealing and quenching to achieve the desired material properties, which further adds on to the energy consumed [2]. To address this, research has begun to explore the use of the solid-state process to manufacture metallic wires as an alternative to conventional wire drawing. Friction Stir Extrusion (FSE) is a promising solid-state process to simplify and reduce emissions from wire drawing [1]. The FSE process begins with discarded machining chips from turning or milling processes and consolidates the chips to form wires through severe plastic deformation. This simplifies the wire-making process, and it is conducted at room temperature and pressure conditions, significantly reducing the energy consumed. However, this process mainly uses discontinuous chips, which often introduce defects and segmentations in the produced wires, especially when extruding thin wires [3]. Thus, this study proposes an alternative solid-state process that uses continuous chips to produce thin wires.

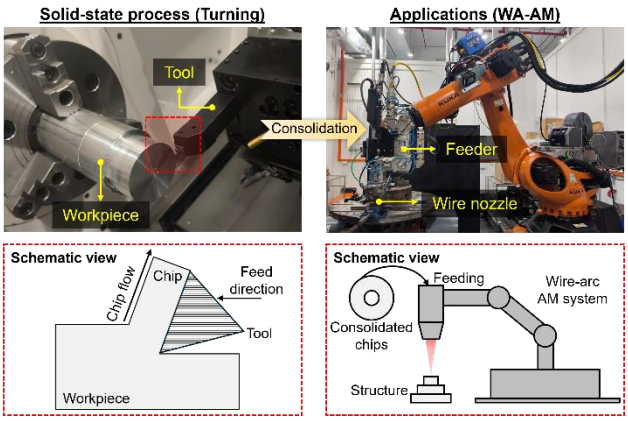

Figure 1. The proposed solid-state process to produce continuous wires and its potential applications.

As shown in Fig. 1, a controlled turning process is used to generate long and continuous chips by varying cutting speed, depth of cut, and tool rake angle. Subsequently, the usability of the chips was assessed through tensile testing. The main focus of this preliminary study is on the turning process, which plays a crucial role in producing defect-free continuous chips suitable for subsequent processing. Continuous chip formation is particularly advantageous, as it minimizes defects associated with inter-chip interfaces when fabricating thin wires. Hence, this work investigates the turning process in detail, with specific attention to chip morphology and the conditions that promote continuous chip formation.

2. Methodology

2.1. Turning process

In this study, all experiments were conducted on a DMG Mori NLX2500 Computer Numerical Control (CNC) lathe machine. The workpiece used was a cylindrical Aluminium 6061-T6 alloy billet with a diameter of 80 mm and a length of 200 mm. The cutting tool consisted of a rhombic carbide insert with a clearance angle of 7° and no chip breaker, referenced as DCMW11T304. Two types of tool holders were used, with a rake angle of 0° and -6°, respectively. The machining parameters used in the experiment are listed in Table 1. The turning experiments were repeated on a fresh workpiece of the same material to ensure reproducibility of the results.

Table 1. Machining parameters for the turning experiments

Machining parameter	Unit	Values
Cutting speed, V_c	m/min	100, 150, 200
Depth of cut, a_p	mm	0.25, 0.50, 0.75, 1.00
Feed, f	mm/rev	0.50
Tool rake angle, γ	°	-6, 0

2.2. Tensile testing, chip characterisation and fracture analysis

Tensile tests were conducted with a universal testing machine, Instron 8501, in reference to ASTM E8/E8M. The chips were aligned with a 40 mm gauge length, and a crosshead speed of 0.6 mm min^{-1} was applied, giving a nominal strain rate of 0.015 min^{-1}. The chip morphology was examined using an Optical Microscope, Keyence VHX-7000. Fractography analysis was performed using Scanning Electron Microscopy (JEOL JSM-IT200) on the fracture surfaces. The surfaces were cleaned with ethanol before imaging. Images were collected from low to high magnification to document the fracture features such as dimples, shear lips, and fracture path.

2.3. Finite element modelling

To enhance the physical comprehension of the formation of machining chips during the cutting of Al6061 alloy, the finite element method (FEM) was implemented. A 2D orthogonal cutting setup, taking reference from Mabrouki et al, was considered to approximate the turning process [4]. The workpiece was modelled using four-node bilinear plain strain elements with reduced integration and enhanced hourglass control (CPE4R), and the tool was modelled as an analytical rigid body. The explicit solver from the Abaqus 2023 software was used to perform the simulation. The workpiece is assumed to behave based on the Johnson-Cook plasticity constitutive material model. This provides a good description of metals undergoing large strains, high strain rates, and thermal softening. The constitutive law is established as follows

$$\bar{\sigma} = (A + B\bar{\varepsilon}^n)\left[1 + C\ln\left(\frac{\dot{\bar{\varepsilon}}}{\dot{\bar{\varepsilon}}_0}\right)\right]\left[1 - \left(\frac{T - T_r}{T_m - T_r}\right)^m\right] \quad (1)$$

Where $\bar{\sigma}$ is the plastic stress, $\bar{\varepsilon}$ is the equivalent plastic strain, A is the initial yield strength, B is the hardening parameter, n is the work hardening exponent, C is the strain rate dependency coefficient, $\dot{\bar{\varepsilon}}$ is the plastic strain rate, $\dot{\bar{\varepsilon}}_0$ is the reference strain rate, T_m is melting temperature, T_r is reference temperature, and m is the thermal softening coefficient. The J-C values and relevant thermal-mechanical properties for Al6061 are listed in the table below.

Table 2. Thermal-mechanical and damage properties of Al6061-T6

Parameter	Values	Parameter	Values	Parameter	Values
Elastic modulus (GPa)	70	A (MPa)	324	D_1	-0.77
Poisson's ratio	0.33	B (MPa)	114	D_2	1.45
Density (kg/m^3)	2700	n	0.42	D_3	-0.47
Melting temp (°C)	660	m	1.34	D_4	0
Specific heat (J/kg °C)	900	C	0.002	D_5	1.6
Thermal conductivity (W/m°C)	237	$\dot{\varepsilon}_0$ (s^{-1})	1	Taylor–Quinney factor	0.9

To model the chip formation process, the Johnson-Cook damage model was used. It is considered that failure will occur when the damage parameter exceeds a critical value, and the element will be deleted. The damage criterion is defined as

$$D = \frac{\bar{\varepsilon}_0^p + \sum\Delta\bar{\varepsilon}^p}{\bar{\varepsilon}_f^p} \quad (2)$$

The increase in equivalent plastic strain, $\Delta\bar{\varepsilon}^p$ is summed at the end of each increment. The equivalent plastic strain for damage initiation, $\bar{\varepsilon}_f^p$ is determined based on

$$\bar{\varepsilon}_f^p = \left[D_1 + D_2\exp\left(D_3\frac{P}{\bar{\sigma}}\right)\right]\left[1 + D_4\ln\left(\frac{\dot{\bar{\varepsilon}}^p}{\dot{\bar{\varepsilon}}_0}\right)\right]\left[1 + D_5\left(\frac{T - T_r}{T_m - T_r}\right)\right] \quad (3)$$

In which D_1 is the initial failure strain, D_2 is the exponential factor, D_3 is the triaxiality factor, D_4 is the strain rate factor, D_5 is the temperature factor, and $P/\bar{\sigma}$ is the stress triaxiality. The corresponding values of the damage constants are also listed in table 2. The friction at the tool-chip interface is also a significant factor in affecting the chip formation process in the simulation. Coulomb's friction law is used in this study, with the coefficient of friction set to 0.3. This value is an acceptable assumption for low- and medium-speed cutting conditions.

3. Results and discussion

3.1. Chip morphology

Machined chips were collected and examined under the optical microscope. The results are summarised in Fig.2. Generally, all the chips formed are long, continuous, and helical. In addition, two main classes of chips were collected: continuous smooth chips and continuous serrated chips. In Fig.2, the red square indicates serrated and the black indicates smooth. It was observed that as the depth of cut increases, serration becomes likely. Moreover, as the cutting speed increases, serration becomes unlikely. Lastly, for a negative rake tool, the appearance of serrated chips becomes more frequent.

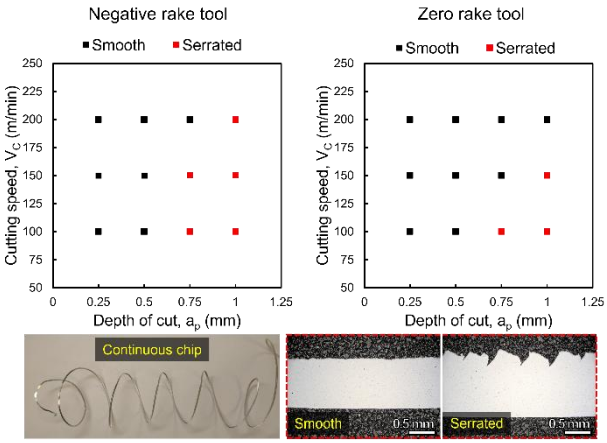

Figure 2. Chip morphology of the machining chips obtained

The fundamental cause of chip serration can be correlated to the adiabatic shear banding (ASB) phenomenon during machining [5]. It is often reported in various literature that cutting speed is the main factor contributing to chip serration and it occurs for high-speed machining, at about 460 m/min for aluminium alloy [6]. However, in this study, serration occurred under moderate cutting speed. This is because in this study, the feed and depth of cut are larger than the usual machining operation to achieve the desired dimensions of the machining chips. Thus, it is more appropriate to evaluate the serration phenomenon based on the collective effects from various machining parameters rather than just focusing on an isolated cutting parameter. Chip serration is governed by the two competing effects: the stabilising influence of work hardening, and the destabilising influence of thermal softening. The Recht criterion can be used to determine the influence of the two effects. The Recht criterion (4) indicates that shear instability occurs when the thermal softening contribution exceeds the strain hardening contribution. Accordingly, the Recht ratio R, when below one, suggests that chip segmentation is likely, and the lower the ratio, the higher the degree of serration [7].

$$\frac{\partial \tau}{\partial \gamma} + \frac{\partial \tau}{\partial T}\frac{dT}{d\gamma} \leq 0 \tag{4}$$

$$R = \frac{\partial \tau / \partial \gamma}{-(\partial \tau / \partial T)(dT/d\gamma)} \tag{5}$$

In equation (4), the first term represents the strain hardening rate, while the second term represents the thermal softening contribution, which consists of material thermal sensitivity and the adiabatic heating rate, respectively. As it is difficult to quantify the terms experimentally for the turning process, these terms are evaluated using FE fields $(\gamma, \dot{\gamma}, T)$ together with the Johnson–Cook constitutive relation. The J-C flow law, when expressed in shear form

$$\bar{\tau} = \frac{1}{\sqrt{3}}\left(A + B\left(\frac{\bar{\gamma}}{\sqrt{3}}\right)^n\right)\left[1 + C\ln\left(\frac{\dot{\bar{\gamma}}}{\sqrt{3}\dot{\varepsilon}_0}\right)\right] \left[1 - \left(\frac{T - T_r}{T_m - T_r}\right)^m\right] \tag{6}$$

Where $\bar{\tau}$ is the plastic shear stress, and $\bar{\gamma}$ is the plastic shear strain. The strain hardening rate and thermal sensitivity can be determined by taking partial derivatives of equation (6). Lastly, in adiabatic conditions, the adiabatic heating term is approximated by as

$$\frac{dT}{d\gamma} = \frac{\beta \tau}{\rho c} \tag{7}$$

In which, β is the Taylor–Quinney factor, ρ is density, and c is the specific heat capacity. By using equation (1), (6), and (7), the respective hardening and softening terms can be computed, and the Recht ratio is computed using (5). The results are summarized in the figure below.

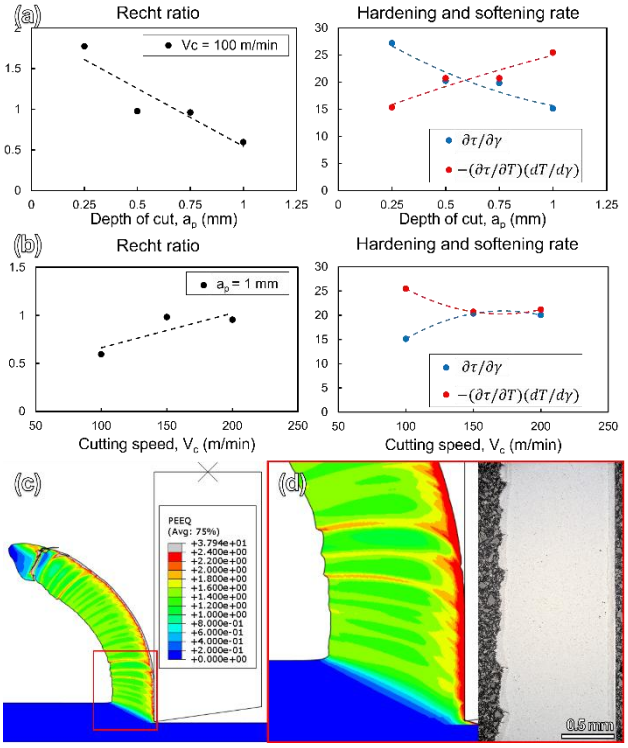

Figure 3. The Recht ratio, strain hardening, and thermal softening rate: (a) Varying ap with Vc = 100 m/min; (b) Varying Vc with ap = 1 mm; (c) FE result showing the PEEQ field; (d) Comparing simulation and experimental results.

It is observed that as the depth of cut increases, the FE simulations predict higher temperatures in the shear zone and along the tool–chip interface, which increases dT/dγ and the magnitude of ∂τ/∂T. Consequently, the thermal softening rate increases with depth of cut, implying that thermal softening becomes increasingly competitive relative to strain hardening and chip serration becomes likely (Fig 3a). When investigating the effect of cutting speed, it was observed that chip serration occurred at moderate cutting speed, whereas the literature reported that chip serration happens at high cutting speed. The results from this study remain consistent with this general trend. As shown in Fig 3b, the Recht ratio peak at 150 m/min and start to decrease at 200 m/min. The decrease in the Recht ratio indicates that thermal softening becomes more dominant at higher cutting speeds, which aligns with prior studies. However, the Recht ratio is well below one for 100 m/min, implying that serration can occur even at moderate cutting speeds when other parameters, particularly depth of cut, promote shear localization. In other words, the influence of depth of cut is sufficiently strong that it shifts the onset of chip serration to lower cutting speeds. Therefore, this result has shown that evaluating the occurrence of chip serration with a single cutting parameter is insufficient, and future studies will conduct more extensive investigations on various cutting conditions and establish a cutting criterion for chip serration under the collective influence of those cutting parameters. In addition, this FE-Recht criterion framework can accurately detect the onset of chip serration. For the case when the Recht ratio is around 0.96, experimental observation also shows slight serration (Fig. 3c,d). The Recht ratio can be used as the critical value in determining the usability of the machining chips. In the following section, this usability is assessed through a tensile test and fractography analysis.

3.2. Fractography analysis

Fractography analysis aids in the establishment of the fracture mechanism by examining the fracture surface. These observations link the material behaviour, such as ductility and toughness, to the machining parameters, and provide empirical evidence to justify the existence of an optimised processing zone for desired chips. By comparing the side profile view along the specimen axis, it can be observed that the smooth chip exhibits cup-and-cone fracture, while the serrated chip shows slant fracture. This can be correlated to the surface defects on the serrated chips. Those sharp edges served as areas of high stress concentrations, promoting the crack to initiate with a lesser load required. The smooth chips showed pronounced necking, indicating substantial plastic deformation and load-carrying capacity prior to fracture. This is further confirmed through examining the chips cross-section. The existence of dimples is concrete evidence of void nucleation and coalescence, commonly observed in ductile materials after exceeding the critical plastic strain. The deep dimples also suggest that smooth chips exhibit better toughness as compared to serrated chips, which show shallower dimples. The equiaxed shape dimples on the smooth chips also suggest that it is a tensile-dominated failure, whereas serrated chips failed dominantly due to shear, leading to the formation of directional elongated dimples.

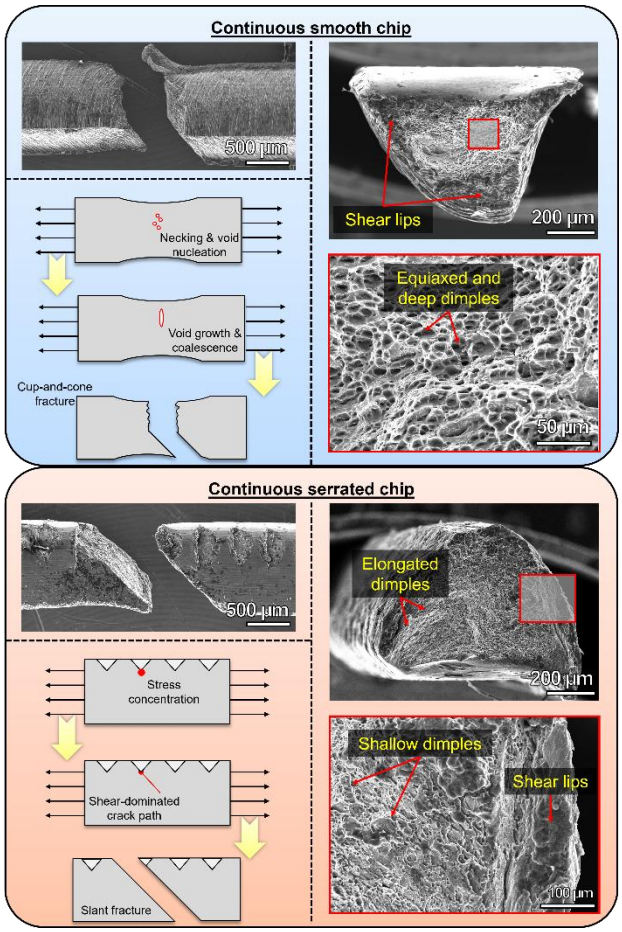

Figure 4. Fractography and fracture mechanism of serrated and smooth machining chips

The fractography analysis suggests that serrated chips will have limited applications and usability due to the reduced ductility and toughness. This part of the study aims to produce machining chips that can be used for further processing and development. In addition, the results also correlate well with the previous findings, in serrated chips, the thermal softening effect localised the strain in a narrow band. As a result, this area is excessively deformed, allowing minimal further plastic deformation, thus showing lowered material toughness and exhibiting shallow dimples on the fracture surface. Therefore, it is clear that chip serration is an undesirable phenomenon, and by careful control of the machining parameters, desired chips can be produced for subsequent processing and forming.

4. Conclusion

In conclusion, this paper presented a feasibility study to produce continuous wires through solid-state processes. As a preliminary assessment, the study identified chip serration as a key factor affecting the quality of wires produced. As shown experimentally, machining parameters affect the type of machining chips produced, as it has an influence on the stabilising and destabilising factors in shear band formation. Whenever the destabilising influence of the thermal softening outweighs the stabilising effect from the work-hardening during plastic deformation, the serration phenomenon occurs. The use of the Recht criterion with FE models to quantify the degree of serration is also presented, showing good agreement between numerical and experimental results. From the fractography analysis, it is evident that chip serration is an undesirable phenomenon, and smooth machining chips with a higher Recht ratio (>0.9) are desirable for subsequent processing and usage. Subsequent studies will first determine the optimum process window for the turning process with the use of the FE-Recht criterion framework. Secondly, to improve the quality of the wires, studies will be conducted to understand if the wires can sustain further deformation and processing to ensure usability. Finally, the usability of the continuous wires produced will be evaluated through their applications in wire-based AM techniques.

Acknowledgement

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