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A novel sample holder for operando X-ray nanoscopy of perovskite solar cells

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Abstract
Synchrotron light sources pose at a unique position for condensed matter science, enabling advances in the characterization of new materials, including frontier research for sustainable energy production. In this work we present the design and first results of a novel precision sample holder for in-situ and operando studies of entire perovskite solar cell devices at the X-ray scanning nanoprobe TARUMÃ, at the CARNAÚBA (Coherent X-Ray Nanoprobe Beamline) beamline at the Brazilian Synchrotron Light Laboratory (LNLS/CNPEM). Harvesting the high-brilliance of the 4th-generation storage ring Sirius, the station, with in-house designed optomechanics and the experimental setup, can perform multi-modal analyses, simultaneously with nano-ptychography coherent diffraction imaging (ptycho-CDI), nano-diffraction (XRD) and X-ray fluorescence (XRF) imaging of the devices, among others. A custom-made thin-film platinum temperature sensor and heater chip deposited at the indium-tin-oxide (ITO) coated borosilicate solar device substrate was developed for temperature control between 24 and 300°C. This chip is then used to assemble the solar cell device. This enables working and process conditions emulation during the X-ray imaging with seamless integration with the solar device manufacturing process. At the beamline, the chip is mounted in a special high-stiffness holder designed for thermal decoupling and position drift reduction. Additionally, irradiation incidence is emulated with a solar-spectrum LED, whereas air humidity is controlled by nitrogen purge with an embedded humidity sensor feedback. All this proved to be compliant with the nanometer-level fast-scanning positioning requirements at the beamline.

Keywords: Synchrotron light sources, renewables, solar cells, perovskite, nanoscopy, X-ray, optomechanics, scanning stages

1. Introduction

Perovskites are a class of materials that have potential in the field of renewable energy, specifically in solar cells due to their high efficiency and low-cost. The TARUMÃ station at the Brazilian Synchrotron Light Laboratory (LNLS/CNPEM) is an advanced facility that can perform multi-modal analyses of samples, including nano-ptychography, XRD, and XRF imaging [1], [2]. The presented development in this paper is a custom-made holder for perovskite solar cells that includes a thin-film platinum temperature sensor and heater in a glass substrate chip, allowing for temperature control between 24-300°C, simulating working conditions during X-ray imaging, allowing to understand the behavior of perovskites under different conditions, which is essential for the development, optimization, and scaling of PSCs technology

2. System architecture

The TARUMÃ motion stage has a magnetic kinematic mount and common electrical and gases interface [2], allowing for fast swapping of different sample holders and enabling multiple techniques and in-situ, operando experiments. The perovskite heating sample holder has the same interfaces, and all active elements, sensors, and harnesses are coupled to the so-called kinematic interface plate (Figure 1.III). Here we further describe the individual systems.

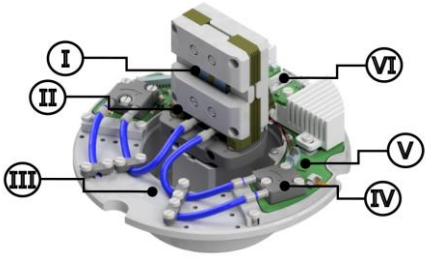

Figure 1. Control Chip (I), Chip Holder (II), Interface Plate (III), Gas Flow Path (IV), Interface Plate PCB (V), and Illumination System (VI).

2.1. Temperature control chip

The temperature control system used in the setup is based on an in-house designed and built 15x15mm glass chip that incorporates two resistive circuits: a heating circuit and a temperature measurement circuit (Figure 2). Both circuits are deposited using photolithography on the non-conductive side of ITO-coated (Indium Tin Oxide), 4-10ohm/m², 1.1mm thickness, borosilicate glass substrate from Delta Technologies, LDT, which is required for the manufacture of PSCs devices. The conductive side is used for the preparation of the solar cell device.

The heating circuit is composed of a nominal room temperature resistance of 100Ω and operates on the principle of the Joule effect, where electrical current is converted to heat as it passes through the conductor. The target resistance was determined through a lumped analysis of the complete holder, which mapped the thermal coupling with the metallic structure and the air through convection. This resistance is sufficient to deliver up to 5W to the substrate with the TARUMÃ 0-24V DC in

house designed power supply [3]. The heat is then conducted through the substrate to the sample, enabling precise temperature control within the required range of 24°C to 300°C. Finite element analysis (FEA) of electrical coupling using ANSYS software was performed on multiple platinum trace geometries to ensure an acceptable and homogeneous temperature within the region of interest of 3x3mm centered at the chip.

The temperature measurement circuit is composed of a nominal 300Ω platinum resistance trace and is designed to behave like an RTD (Resistance Temperature Detector), with a resistance that varies according to the temperature. The dimensioning and trace geometry were designed using the same methodology as the one applied for the heating element. The expected resistance R to temperature T dependence is described by Equation 1, where R_0 is a chip-specific coefficient and A and B are constants that describe the chip's behavior [4] and are input parameters for the TARUMA´s temperature controller [5]. For platinum RTDs a linear behavior is expected, being R_0 the most critical dominant parameter that can vary due manly due to film thickness variation or lithography inaccuracies.

Equation 1. Callendar-Van Dusen equations

$$R = R_0(BT^2 + AT + 1)$$

The manufacturing of both circuits was based on a lithography process using RF-magnetron sputtering. The steps are briefly summarized below:

1. Laser stencil photolithography mask printing,
2. Deposition of adhesion promoter (hexamethyldisilazane) and photoresist (Shipley, S1811) on a large 50x50mm (3x3 array of chips) glass-ITO substrate using spin coating,
3. Engraving the pattern using UV exposure (300nm) through the photolithography mask,
4. Removal of excess photoresist using a washout process,
5. Substrate oxygen plasma cleaning to improve adhesion,
6. Deposition of a Chromium (Cr) layer with a thickness of 20 nm using RF sputtering,
7. Deposition of a platinum thin film with a thickness of 200nm using RF sputtering,
8. Removal of photoresist by washout process (MIF 312),
9. Dicing of the individual chips,
10. Stress relief by thermal treatment (300°C, 30 minutes) of the metallic film.

The last step was proven to be crucial for the correct functioning of the temperature sensor circuit as the annealing of the chip reduced the RTD traces resistivity by about 28% as shown further. After all the steps for the glass chip manufacture, the PSC can be manufactured on the opposite substrate side by multiple different routes. Finally, the anode and cathode gold electrodes are deposited over the PSC by vacuum thermal evaporation. The final organization of the device can be seen in Figure 2 (a). Figure 2 (b) presents a manufactured chip.

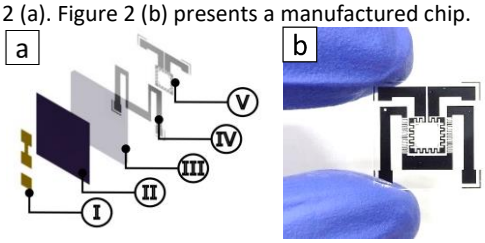

Figure 2. (a) PSC top gold electrodes (I), PSC (II), glass substrate (III), heater platinum traces (IV), and temperature sensor platinum traces (V). (b) Picture of the actual glass chip with heater and sensor traces.

To verify the performance of the temperature control system and to determine the individual chips Callendar-Van Dusen parameters, two parallel projects were developed: a characterization device and the final holder for the beamline application. These projects allow for the experimental testing of the system and its behavior under different conditions.

2.2. Chip holder

The chip holder was designed using principles of precision engineering to thermally decouple the chip from the TARUMÃ surroundings while ensuring high mechanical stiffness and providing the necessary connections to control and operate the chip. To achieve this, a custom Ti64 flexure-based holder was created (Figure 3.a.III). The holder works by using the alloy low thermal conductivity and a thin flexure cross section to create a low thermal conductivity path from the chip support to its frame, minimizing heat leak to the rest of the structure. This allows the chip to be maintained at the desired temperature with minimal power and reduces parasitic drifts.

In complement, the flexure's weak-direction stiffness was designed to allow the glass substrate to expand due to thermal effects with minimal reaction force, inferior to 3N. This is important because the chip is held in place by four spring-loaded clamps that rely on friction forces to prevent slip-stick behaviors that could misalign the PSC features during beamline measurements.

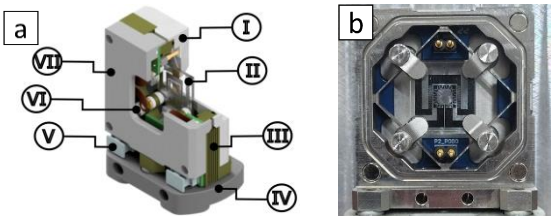

Figure 3. (a) Chip holder mount section with front magnetic cover (I), glass chip (II), Ti64 frame (III), kinematic holder mount (IV), MOLEX connectors (V), spring loaded clamps (VI), and back magnetic cover (VI). (b) Picture of the chip holder.

The holder was also designed to make it easy to exchange the chip by using spring-loaded clamps (Figure 3.a.VI), snap-in magnetic interfaces for the covers (Figure 3.a.I and a.VII), and a magnetic kinematic interface (Figure 3.a.IV) for coupling with the interface plate (Figure 1.III). This allows the user to bring only the holder to the bench for cell swapping without removing the entire interface plate from the TARUMÃ's motion stage.

To efficiently route signals and save space, the CARNAÚBA's sample holders often utilize printed circuit boards (PCBs) for both electronics assembly and signal harnessing. For the temperature sensor and heater traces on the glass chip, contact is made using four treaded pogo pins placed at the fixation points beneath the spring-loaded clamps (Figure 4.a.I). These are connected to an intermediate PCB using thin copper stripes (Figure 4.a.III).

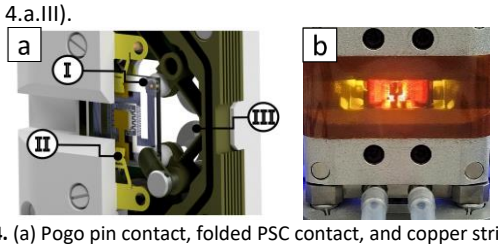

Figure 4. (a) Pogo pin contact, folded PSC contact, and copper stripe harnessing. (b) Picture of the holder with Kapton sealed cover.

The PSC contacts, used for junction measurements of the cell, are contacted by a pair of custom flat spring contacts (Figure 4.a.II) in addition to pogo pins soldered an intermediary PCB. All signals are then routed to a larger PCB at the Interface Plate (Figure 1.V), which is responsible for routing signals from the chip holder and LED system to a common exit connector for a

LEMO patch panel at the TARUMÃ. All PCB connections utilize MOLEX PICOBLADE series connectors.

One key variable for scientific cases studies of the degradation of PSCs is the atmosphere composition and humidity [6]. In this sense, the holder incorporates a loop channel (Figure 1.IV) and an optional sealed compartment (Figure 4.b) surrounding the chip where inert gases can be flushed. Two analog humidity sensors model HIH-4031-001 by Honeywell were embedded in the tabletop interface PCB and measures the gas humidity in the entrance and exit of the holder. The gas composition and flow rate can be controlled by the TARUMA's gas infrastructure.

2.3. Illumination system

The sample holder's illumination system employs a single broadband SMD LED light source SMBBIR45A-1100-02 from USHIO Optics (Figure 5.a.II). This LED has a spectrum distribution that is closer to the solar spectrum than most ordinary white LEDs and offers a high degree of directivity, meaning that most of the light is directed towards the target. This helps to achieve the minimum power required to produce an irradiance of one sun on the surface of the solar cell while minimizing the illuminated area. For the 3x3mm target perovskite area, this equates to 14mW.

The LED light is directed to a small mirror (Figure 5.a.III) which reflects the light onto the sample trough a small mask (Figure 5.a.IV). This setup allows control of the illuminated area, with the ability to vary the shape and size of the region by adjusting the position of the LED, mask, and mirror. The emitted spectrum was measured with an Ocean Optics QEPro-ABS spectrometer and showed a strong blue peak at 450nm, but an acceptable overall distribution above 500nm (Figure 5.b). Future developments will include the use of filters for better solar simulation. The cooling relies on natural convection and is ensured by EDM machined aluminum fins (Figure 5.a.I). The module's electrical connections are also redirected to the Interface PCB.

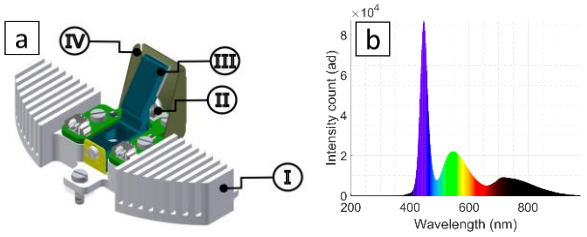

Figure 5. (a) Final design of the lighting system and its components: heat sink (I), LED source (II), flat mirror with flexure system (III), and mask (IV). (b) Measured UV-NIR LED emission spectrum.

3. Chip characterization

To characterize the chip behavior before the final sample holder fabrication, a 3D printed test setup was manufactured (Figure 6.a) with a Form3 3D printed in clear resin. Pogo pins were used for electric contacts with the chip (Figure 6.a.II) and wired to jack connectors (Figure 6.a.III) [7]. The chip was characterized by providing power steps to the heating circuit with a Keithley 2280s benchtop supply. The temperature was measured using an InfraTec ImageIR 8300 thermal camera as shown on Figure 6.b. This method was chosen because it is less invasive than using a physical sensor, which would be limited by space constraints and could affect the results due to the mass of the component influencing the thermal inertia of the system. The variation of RTD circuit was monitored using an Agilent 34410A benchtop multimeter. The thermal cycles were executed such that a maximum current was reached, after which decreasing steps were applied until the initial current value was reached.

To monitor the temperature using the thermal camera, a region of interest (3x3mm, solar cell area) on the substrate was defined, where the average temperature would be evaluated at each time step with custom Python scripts. A thin carbon tape was glued on the opposite substrate side to increase the thermal emissivity and allow a correct absolute temperature measurement [8].

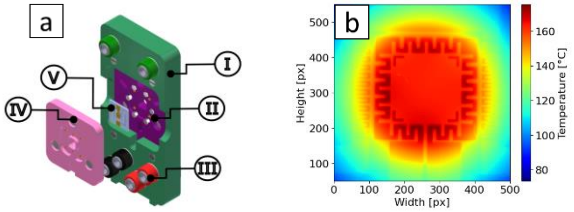

Figure 6. (a) 3D printed holder (I), pogo electrical contacts (II), electrical jacks (III), magnetic cover (IV), and glass chip (V). (b) Temperature map of a chip.

Hysteresis characterization was carried out by examining the trace resistance of the sensing chip as a function of temperature in multiple cycles. The initial results showed that the device exhibited high hysteresis, as the equivalent resistivity tended to decrease after exposures higher than 100°C. This behavior is undesirable for accurate temperature control and absolute measurement, so the phenomenon was further investigated. The hypothesis was that the thin metallic platinum film experiences high residual stresses due to the PVD process, which affects the film's conductivity. When the temperature exceeds a certain threshold, stress relief occurs, and the film's resistivity decreases. This hypothesis was tested by preheating the chips up to 300°C for 30 minutes in a hot plate to induce strain relief. Figure 7.a shows the electrical resistance versus temperature plot of 3 consecutives heating cycles for a chip labeled B6 where it was noted a reduction of resistance after the second cycle when the temperature surpassed 100°C. Figure 7.b shows the same for a chip F2 that was treated with the stress relieving method and presented no resistance variation after each cycle. Before and after resistance values for multiple chips are shown on Table 1.

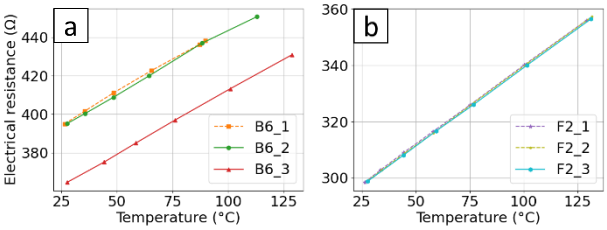

Figure 7. (a) Electrical resistance versus temperature of a chip labeled B6, for heating cycles 1 to 3. (b) Same for a chip labeled F2.

Table 1. Chip temperature sensing traces resistance before and after heating cycles.

CHIP ID	RESISTANCE (OHM, BEFORE TREATMENT)	RESISTANCE (OHM, AFTER TREATMENT)	PERCENTUAL VARIATION
D2	418.21	296.19	-29.18%
D3	440.9	318.49	-27.76%
D4	426.6	305.02	-28.50%
D5	423.1	306.66	-27.52%
D6	430.5	311.13	-27.73%
D8	441.79	320.6	-27.43%
D9	450.22	324.5	-27.92%
AVERAGE	**427.9**	**307.5**	**-28.14%**
STANDARD DEVIATION	**7.7**	**7.3**	**0.62%**

4. Beamline measurements

To commission the final setup and present its capabilities to CARNAUBA's users, a test campaign was executed in November 2022 (Figure 8.a). During that, XRF and XRD measurements were

performed with the TARUMÃ monochromatic beam in fly-scan mode.

4.1. Position stability

To evaluate the position stability of the chip during the heating phase, a thin 2D sample made of a hybrid organic-inorganic perovskite (HOIP) was used as a target during a temperature ramp up to 150°C. It has microscale features in its morphology ranging from 1 to 5µm and lengths from a hundred to a few hundred micrometers [9] that can be used as reference tracking marks in XRF maps (Figure 8.b), allowing for the calculation of displacement between scans by cross correlation technique. This method was already used at TARUMÃ by [10].

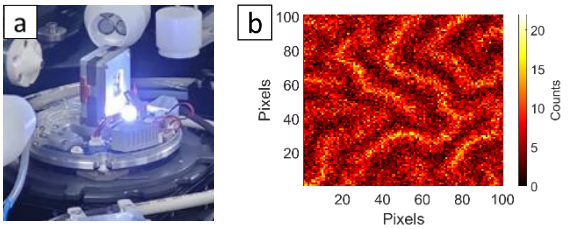

Figure 8. (a) Final setup at TARUMÃ. Example of XRF 2D map used for chip position tracking.

Figure 9 shows the accumulated displacement of the chip for a full heating and cooling cycle and demonstrates a maximum 4µm displacement in the Y direction in the full test temperature range – which is compatible with the PSC scientific feature sizes, allowing a full temperature range device microstructure characterization and validating the efforts on mitigating undesired displacements using precision engineering principles. The chip temperature instability was no larger than 0.1 °C during the test.

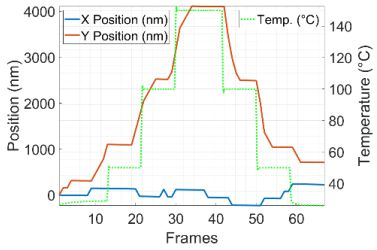

Figure 9. In-plane HOIP sample accumulated displacement plot versus temperature.

4.2. Scientific results

The complete setup (Figure 8.a) has been used to obtain the nano-XRD maps in complete devices up to this date. This technique allows obtaining the spatial resolved lattice parameter of the perovskites and then calculating the strain variation of the structure inter-grain or in individual grains. The strain is directly related to several properties of the perovskites, such as stability, bandgap, band position, and activation energy of ion migration.

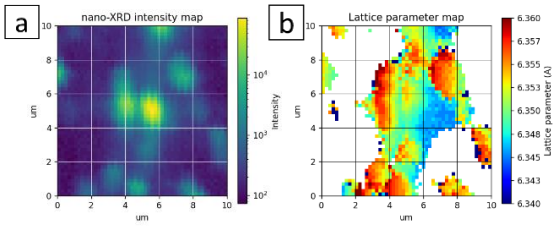

Figure 10. (a) Nano-XRD intensity map of complete PSC device obtained at 10 keV in reflection mode. (b) Respective lattice parameter map.

Figure 10.a shows an intensity nano-XRD map of a $CsFAPbI_3$ perovskite in a complete device (ITO/SnO_2/Perovskite/Spiro-MeOTAD/Au) in reflection mode obtained at the energy of 10 keV. The map shows the existence of the perovskite grains with around 2µm. Grains with different tilting orientation in relation to the area detector appear without signal in the nano-XRD map. Figure 10.b shows a lattice parameter map of the same region, revealing a variation in the grains that are under investigation.

5. Conclusion

A new in-situ, operando experimental setup was designed and built for the TARUMÃ station, enabling new possibilities on perovskite solar cells characterization and development. Using micro-fabrication techniques, a glass chip was developed to heat and measure the sample temperature up to 300°C and was characterized and used for scientific experiments. A miniaturized holder was also developed for thermal decoupling of the chip while ensuring mechanical stability, low position drift and embedded electrical connections. Also, a gas-flow system and an illumination source were incorporated to allow extra environmental emulation. Overall, the tests presented consistent results, with reliable chips and stable, continuous holder operation. Finally, the setup was used at TARUMÃ for XRF, nano-XRD and lattice parameter maps calculation of a HOIP sample.

Acknowledgements

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