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ITRS roadmap is pushing wafer handling to milli-Kelvin performance

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Abstract

The recently redesigned wafer handler module for ASML's latest NXT scanner and future scanners is able to condition a wafer in the milli-Kelvin range at 15% increased productivity. All sources of thermal disturbance are controlled. In the vicinity of the wafer, dissipation sources are removed or shielded, clean air is temperature and flow controlled and heat radiation is limited. The silicon wafer itself is conditioned on 2 water cooled burl tables. The conditioning tables are placed in series to maximize the throughput. The result is a 5 times improved thermal performance of wafer handler at increased throughput.

Keywords: wafer handling thermal conditioning milli kelvin overlay

1. Introduction

The next overlay nodes in the Semicon industry require more accurate control of the thermal expansion of silicon wafers before expose in a lithography scanner. This makes accurate thermal conditioning of the wafers a necessity.

Wafer handler (WH) is the module in an ASML scanner between the Track and the Scanner expose chucks. Wafer Handler performs 3 basic tasks: wafer transport, wafer positioning and wafer thermal (pre-)conditioning.

The new wafer handler module called WH Mk7 is designed by VDL ETG in close cooperation with architects and designers from ASML, Sioux CCM and Demcon. Sioux CCM is responsible for project management and system architecture, Demcon designed the new wafer pre-aligner module, and VDL added manufacturing technology . In addition, VDL ETG is responsible for the WH product during its full life cycle. Two proto wafer handlers Mk7 are already delivered in 2016 to ASML. VDL ETG will start pilot production in 2017.

In this paper the redesign of the wafer handler is presented in chapter 2. In chapter 3 the qualification tooling is discussed, followed by the measurement results of wafer handler in chapter 4. Chapter 5 is the summary.

2. Design of the Wafer Handler Mk7

The redesign of the wafer handler is initiated to improve the thermal performance of the wafer load path to the expose chucks in the scanner. A thermal model of the wafer handler was used to give direction to the redesign.

In the thermal model, sensitivities for the following thermal disturbances are taken into account: 1.Wafer input temperature, 2.Environmental temperature, 3.Clean air supply temperature, 4.Wafer throughput variations and 5.Air from the expose stages compartment.

The major performance requirements for the wafer handler are summarized in Table 1.

Table 1 : Major performance requirements for Wafer Handler

Performance	Requirement
Wafer diameter	300 mm
Throughput improvement	+15%
Input wafer temperature range	22 +/- 1 C
Average wafer temperature repro 3σ	< 4 mK

The redesign of the wafer handler includes a new pre-aligner, thermal shielding and an air shower above the wafer load path, see Figure 1.

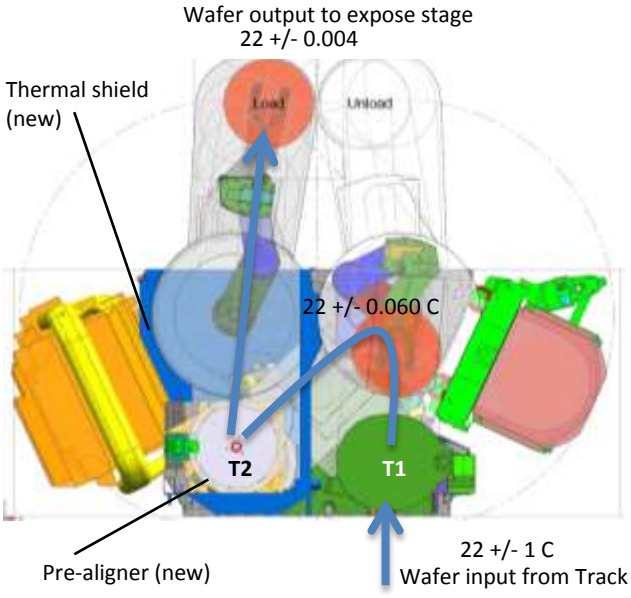

Figure 1. Wafer Handler layout with 2 conditioning tables T1 and T2. The wafer flow is indicated with the blue arrows.

2.1. Pre-aligner with burl table

The previous generations of wafer handlers use a water cooled table in the pre-aligner with an air bearing between the wafer and the table. The advantage of this concept is that the air bearing allows wafer rotation and displacement for pre-alignment in parallel to thermal conditioning. However, the thermal conditioning performance of an air bearing is limited due to the relative large energy effects of expanding air and vacuum extraction in the air bearing under the wafer.

The new wafer handler uses a water cooled table with the wafer in contact with the table by vacuum clamping. This thermal conditioning concept is as accurate as the water temperature through the table. A wafer temperature stability of < 1 mK is achieved for the new pre-aligner.

2.2. Thermal shielding

The next big improvement is the thermal isolation of the wafer load path after the pre-aligner, including a low velocity air shower with down flow. The thermal shielding isolates the wafer load path from the environment. A low velocity air shower above the wafer load path minimizes the thermal disturbance of the wafer and keeps the load path at a stable temperature with respect to the pre-aligner table.

3. Qualification tools

Special qualification tooling is made to verify the sensitivities of wafer handler for the 5 sources of thermal disturbance mentioned in section 2. The wafer handler that was first built, was qualified in this tooling, see Figure 2.

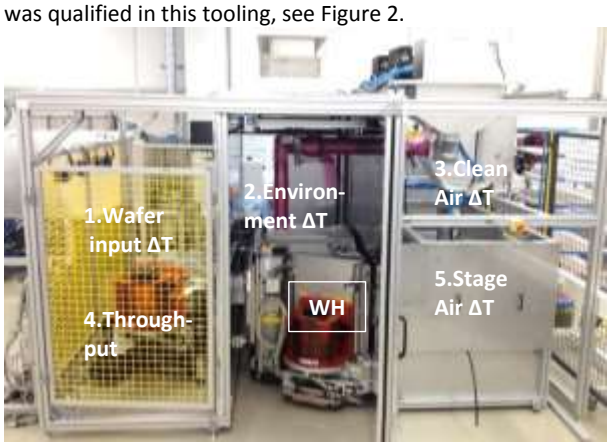

Figure 2. Wafer Handler (WH) in the qualification tooling, with the 5 sources of thermal disturbance.

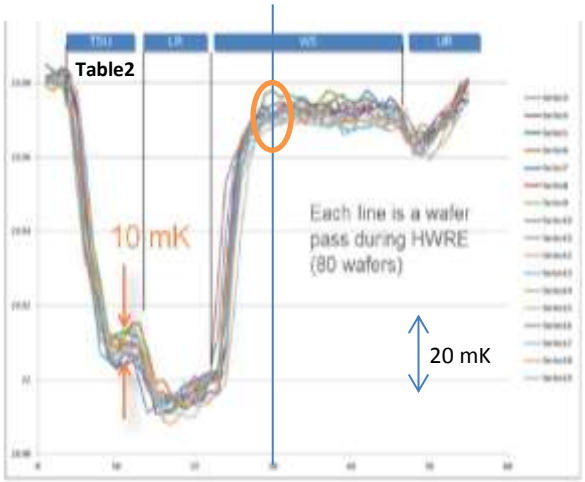

Figure 3. Wafer conditioning result of Wafer Handler Mk5 (current design). The conditioning on 'SU Table1' is not depicted in this figure. The orange ellipse is the wafer load to the expose chuck.

3.1. mK-wafer temperature logger

The main work horse in the sensitivity measurements is a custom designed measurement wafer with 63 very accurate temperature sensors, see Figure 4 and [1] for more info. The measurements wafer is cycled 20 times in-line with ordinary wafers in a normal wafer handling cycle. The temperature readings of the measurement wafer at load to the expose chuck are used to qualify the thermal performance of wafer handler. This measurement series is repeated for different settings of the 5 sources of thermal disturbance.

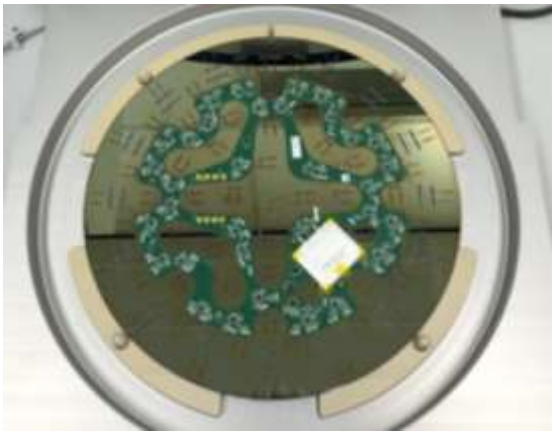

Figure 4. The wireless mK-wafer temperature logger tool

4. Wafer Handler results

The new wafer handler conditions wafers 5 times more accurate at 15% higher productivity than the currently used wafer handler module, compare Figure 3 and 5. The thermal performance of the new pre-aligner module is better than 1 mK, see Figure 5, the temperature at the end of PA Table2.

5. Summary

The performance of wafer thermal conditioning is 5 times improved by the new wafer handler. The sensitivity of wafer handler for different sources of disturbance is measured successfully. The high accuracy of the wireless mK-wafer temperature logger tool [1] has proven to be essential for understanding of the thermal behaviour.

References

[1] Tas M, et al 2017 Euspen Hannover Abstracts ***ICE17328***

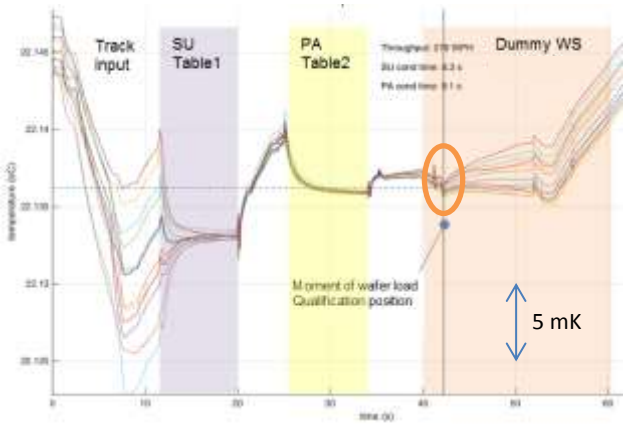

Figure 5. Wafer conditioning result of Wafer Handler Mk7 (new design) using the mK-wafer tool for different Track input temperatures. Note that the scale is 4x smaller than in the left figure!