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Dicing by “Crack-and-Fracture” – Novel separation method for MEMS substrates

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Abstract

The dicing of microsystems is an essential part of the batch production of MEMS. For this purpose, various methods have been developed, improved and integrated into a highly productive process. The future challenges of the batch manufacturing in this part are the 3-D integration of individual chips, the increasing diameter of the substrates and the associated wafer thickness. The establishment of 12" and 18" substrates into MEMS production bring new challenges to all currently used separation manufacturing processes. In this work the established separation process of dicing is evolved. Here, a "Crack-and-Fracture" method for silicon and borosilicate glass (Pyrex®) is examined.

The work shows a novel process for backside chipping-free separation of silicon and glass substrates for MEMS. A theoretical coupling between "Crack-and-Fracture" and the stress intensity factor/crack propagation via the “Paris-Erdogan” law is determined. The area of linear expansion cracks is the active process mode of this method. In order to avoid the areas of subcritical crack growth (no separation) and overcritical crack growth (backside chipping), a high process understanding/control is needed.

Dicing, Crack propagation, Separation, Silicon, Borosilicate

1. Introduction

The separation of substrates into individual segments (chips) is a necessary process step for the production of micro components, which were produced in batch production. An analysis of the state of the art revealed a wide range of existing methods in competition with conventional mechanical separation processes. A known alternative method for classical dicing is laser dicing. In this method, chips are separated by laser radiation to minimize cutting edge breakouts, so-called chipping. The laser dicing processes can be divided into four groups:

- Laser Full Cut
- Lasers using an intermediate layer on the underside of the substrate
- Water-jet-guided laser
- Stealth-Dicing

All the above-mentioned methods [1, 2, 3] produce increased roughness on the sidewall of the chip, require a substrate material adjustment of the laser radiation, and are limited to a maximum of 300 µm thick substrates due to decreasing productivity. In the case of thicker substrates, the processes become too time-intensive and thus too expensive [4].

Evertsen et. al. describe in [5] how a gallium arsenide (GaAs) substrate (light-emitting diodes) is separated with laser and at some point, the laser process and attention has to be paid because of the decreasing cutting quality and productivity [6].

Besides the laser beam-based methods described above, there are a variety of mechanical processing methods. A division is made using the following procedures:

- Scribing and cleaving
- Dicing
- Dice before Grinding / Etching (foil as a functional material for electrical conduction, handling, stabilization, etc.).

In general, it should be note with the described non-mechanical-dicing methods, with a substrate thickness of 300 µm, they feature higher economic disadvantages compared to conventional, mechanical dicing.

2. Experimental

2.1. Dicing

The dicing was done on a dicing machine DAC551. The most important influencing factors were feed rate, material and cutting depth. Fig. 1 shows the dicing assembly, which enables the movement of the chips onto a plastic, soft adhesive tape (blue tape, SWT 20+R Nitto Denko) and the suggested correlation between no separation ($<K_o$), Crack-and-fracture ($K_0>x<K_{ic}$) and uncontrolled cracking/cleaving ($>K_{ic}$).

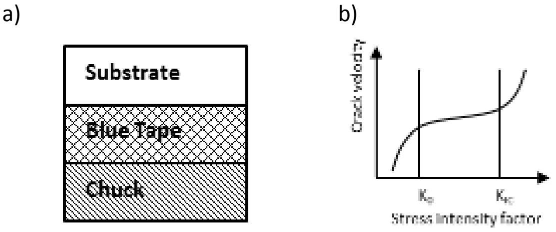

Figure 1. a) Sandwich structure of the dicing assembly and b) approach to the “Paris-Erdogan” law [7]

The dicing process parameters feed rate and the depth of cut as a function of the substrate thickness were varied. The feed rate was increased to 20 m / s and the percentage depth of the cut was increased from 80% to 95% of the substrate thickness. Due to the high fed rates, a hard dicing blade binder is preferred. In order to elaborate a material relationship, a silicon wafer [100] with a thickness of 525 µm and borosilicate glass of the same thickness were tested. The blue tape thickness (60 µm), its properties (adhesive strength, extensibility, etc.), the speed and the cutting edge of the dicing blade have been assumed to be constant. Here, a commercial hub-type abrasive blade with a thickness of 30 µm and a grain size of 2-4 µm was used.

2.2. Characterization

The generated separation sections were examined by means of confocal microscopy, scanning electron measurement and optical control for separation. By means of confocal microscopy, the side walls of the separated chips, the front- und backside-chipping can be characterized.

3. Results

The results show that from a certain cutting depth in combination with increased feed a self-separation takes place. In doing so, the blue tape deforms minimally and a gap to the backside can arise. Fig.2 a shows a cross sectional view into the cutting process and it shows, the separations works without cutting into the blue tape. In Fig. 2 b the SEM image of the resulting substrate material is shown.

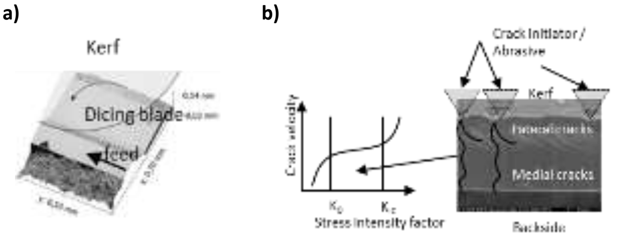

Figure 2. a) Cross section of the crack and fracture process b) Consequence of crack formation and separation

A stable process occurs when the lateral cracks do not reach the blue tape. These cause the backside chipping. By specifically maximizing the process forces in the vertical direction, the medial cracks are prolonged. These ensure the separation. The blade shape of the dicing blades and the laterally acting cutting forces ensure a short-term stretching of the blue tapes. Furthermore, it can be seen that single abrasives in the dicing blade serve as a crack initiator, but the hard nickel binder of the dicing blade has a positive influence on the vertical cracks and reinforces the vertical force. Fig. 3 shows the analyzed chipping on the front- and backside. A moderate acceptable chipping on the frontside is shown, but no chipping and a minimal gap at the backside (< 3 µm).

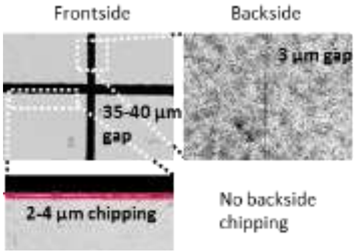

Figure 3. Analysis of the front side and backside chipping silicon

The transition from K_0 to a stability crack propagation is very discontinuous. In this case an unintentional separation due to handling can not be excluded. If the critical fracture toughness K_{ic} is exceeded, the lateral cracks reach the backside and generate chipping (Fig. 4).

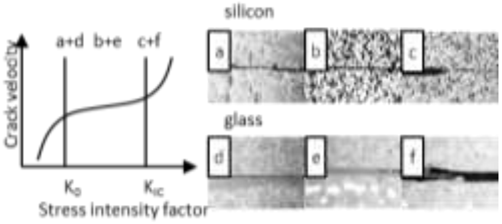

Figure 4. Classification into modes of separation

The higher the feed rate could be chosen, the broader the area of the breaker depth, which leads to crack and fracture. For silicon, a range of 85-95% of the cutting depth could be determined, for glass a range of 90-95%.

4. Concluding marks

The conclusions from the preliminary work are summarized as follows:

- Process through "Crack-and-Fracture" leads to separation during the process without backside chipping
- Process is not dependent on the preferential direction of the substrate (monocrystalline silicon, amorphous glass)

In the next step, the influence of the blue tape will be varied since there is high development potential for increased strain and change in adhesive force. Furthermore, the interaction of the mechanical properties of abrasive, substrate and dicing blade binder should be investigated more closely. In order to more closely coordinate the relationship with the “Paris Erdogan” law, the effective material characteristics (substrate, blue tape, dicing blade, abrasives), such as hardness and modulus of elasticity, and generated lateral and vertical forces, have to be determined [8].

$$K_{ic} = \sigma * \sqrt{\pi * a} * Y$$

$$\sigma = \left(\frac{2 * E * \gamma}{\pi * a}\right)^{\frac{1}{2}}$$

K_{ic}	Fracture toughness
σ	Tension
π	Pi
a	Critical crack length
E	Young´s modulus
γ	Surface damage factor
Y	Geometry factor

A new separation mechanism for the in-situ separation without backside chipping can be used by existing tools and increased process knowledge in the future. A 100 nm thick gold seed layer could be separated in the first tests by "Crack-and-Fracture". A few µm thick electroplated copper layer (e.g. for electroplated layers on the wafer edge) could be separated to a thickness up to 5 µm, but with higher inaccuracy. This is caused by the increased ductility of the metal layer and is further investigated.

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