

Flattening of single crystal SiC by combination of anodic oxidation and soft abrasive polishing

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Abstract

To realize the high efficient and ultra precision flattening of single crystal, CVD grown and reaction sintered silicon carbide (SiC), we are now developing the electro-chemical mechanical polishing (ECMP) process which combines anodic oxidation and abrasive polishing. Ceria (CeO₂) slurry is used as the electrolyte as well as the polishing media. Direct current voltage is in charged between SiC substrate and Pt electrode where SiC played as the anode. Anodic oxidation occurs on the surface of SiC. The oxidation products, mainly SiO₂, have a very low hardness compared with SiC. So the oxide layer is removed by CeO₂ slurry polishing. With the rotation and scanning of the polishing head, anodic oxidation and abrasive polishing are simultaneously conducted. It is found that the balance between the anodic oxidation rate and the polishing rate of the oxide greatly affect the surface quality after ECMP. With a high relative speed of the polishing pad and wafer, polishing rate is higher than the oxidation rate, and a smooth and scratch-free surface can be obtained. In contrast, with a low relative speed of the polishing pad and wafer, polishing rate is lower than the oxidation rate, an oxide layer remain on the polished surface and many scratches, which deteriorates the surface roughness, are introduced to the surface of the oxide layer. It is proved that for the obtaining of a smooth surface by ECMP, the conditions under which the polishing rate is higher than the oxidation rate are necessary.

Silicon carbide, electro-chemical mechanical polishing, roughness, scratch

1. Background

Single-crystal silicon carbide (SiC) is considered one of the most promising next-generation semiconductor materials owing to its excellent properties, such as high hardness, wide band gap, and high thermal conductivity. To realize the highly efficient polishing of single-crystal SiC with minimal subsurface damage, we are now developing a ceria-slurry-based electro-chemical mechanical polishing (ECMP) process, in which anodic oxidation and soft abrasive polishing are efficiently combined [1-3]. Ceria (CeO₂) slurry is used as an electrolyte for anodic oxidation as well as a polishing medium to remove the oxide layer. Since oxidation and polishing are simultaneously conducted, a high material removal rate (MRR) is expected. Also, since CeO₂ abrasive is very soft compared with SiC, the polishing process will only remove the oxide layer without introducing any scratch and subsurface damage. Thus, a flat surface without crystallographical defects is expected with the application of ceria-slurry-based ECMP.

In our previous research, it was proved that localized ECMP was very useful to obtain a scratch-free SiC surface. In this study, whole surface polishing using ECMP was applied to a 4H-SiC wafer. The relationship between the balance of oxidation rate and removal rate in ECMP and the surface morphology after polishing was investigated.

2. Experimental setup of ECMP

Fig. 1 shows the experimental setup of ECMP used for our preliminary research. A 2 inch 4H-SiC substrate is immersed in CeO₂ slurry. The reference electrode (Ag/AgCl) is located near to the specimen so that the potential of the slurry-SiC interface can be controlled. Anodic oxidation occurs on the surface of

SiC. With the rotation of the polishing pad and the specimen, the anodic oxidation of SiC and the removal of the oxide layer are simultaneously conducted. Commercially available single-crystal 4H-SiC substrates (on-axis, n-type), with a specific resistance of 0.10 Ω·cm are used in this work. All experiments are conducted on the Si (0001) face. Commercial CeO₂ slurry used for glass polishing with a concentration of 2.5 wt% is used in ECMP and its pH is 9.24. The electrical conductivity and pH of CeO₂ slurry is 174 mS/m and 11.5. The average diameter of the CeO₂ abrasive particles in the slurry is 190 nm. Before ECMP, the SiC specimen is lapped by diamond abrasives. The load during ECMP is 1350 g. A constant potential of 6.5 V is applied. To adjust the balance of oxidation and polishing in ECMP, the pad rotation speed and wafer rotation speed are adjusted in ECMP.

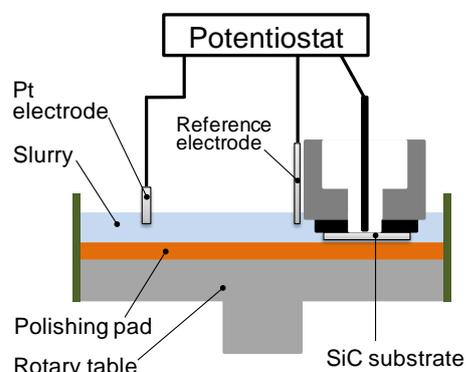


Figure 1. The experimental setup of CeO₂-slurry-based ECMP.

3. Results and discussion

It is considered that the balance of surface oxidation and abrasive polishing in ECMP greatly affect the surface

morphology, such as roughness and scratches, of polished SiC. Therefore, the rotation speeds of the polishing pad and wafer are changed in ECMP experiments to adjust the balance between oxidation and polishing.

Figure 2 shows the changes of current in ECMP along with the elapsed time. When the rotation speeds of polishing pad and wafer were 70 rpm and 150 rpm respectively, the current during ECMP was 0.9 mA and kept constant. Decrease of the current did not occur even at the initial stage of ECMP. It means that the polishing rate was higher than the oxidation rate. After we decreased the rotation speeds of polishing pad and wafer to 30 rpm and 45 rpm, the current during ECMP firstly decreased and then kept constant at 0.7 mA. It means that in the initial stage the oxidation rate was higher than the polishing rate, therefore an oxide layer gradually grown on the surface and decreased the current. Then the oxidation rate gradually decreased and became equal to the polishing rate when the current was 0.7 mA. Thus, it was assumed that there was an oxide layer on the polished surface and this will be confirmed in our future research. When the polishing pad and wafer didn't rotate, only anodic oxidation occurred on SiC surface. As it was shown in Figure 2, the current gradually decreased along with the oxidation time. This is owing to the growth of the oxide layer, which increased the resistance and decreased the current. These results proved that the balance of oxidation and polishing in ECMP could be adjusted by changing the relative speed of the polishing pad and wafer.

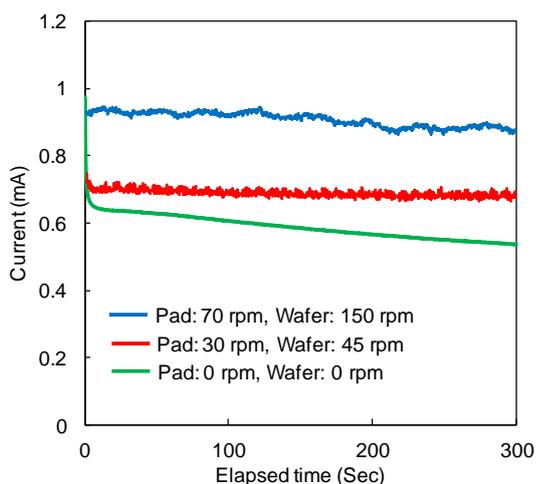


Figure 2. Changes of current of ECMP with different rotation speeds of the polishing pad and wafer.

Figure 3 shows the scanning white light interferometer (SWLI) images of the ECMP polished SiC surfaces. Figure 3 (a) shows the surface lapped by diamond abrasives. Many scratches were introduced. When this surface was processed by ECMP with a high relative speed of the polishing pad and wafer, a flat surface was obtained as shown in Figure 3 (b). As it was previously discussed, the oxidation rate was lower than the polishing rate. Therefore, when an oxide layer was generated, it was immediately removed by abrasive polishing. X-ray photoelectron spectroscopy (XPS) measurements of this surface was conducted which proved that no residual oxide layer on this surface. CeO₂ was very soft compared with SiC, so no scratches could be introduced to the surface of SiC. Thus, a scratch-free surface was obtained.

Figure 3 (c) shows the surface processed by ECMP with a low relative speed of the polishing pad and wafer. A rough surface with many scratches was generated. As it was previously introduced, an oxide layer assumed to remain on this surface. In our previous research, it was proved that the anodic oxide

layer (SiO₂) was very soft [2]. So, many scratches were introduced to the surface of the oxide layer which led to a rough surface.

In our previous research, it was proved that anodic oxidation was a less uniform oxidation process than water vapor plasma oxidation and thermal oxidation [4]. Therefore, it is necessary to remove the anodic oxide layer in the initial oxidation stage in order to obtain a smooth surface. The results of this work prove that for the obtaining of a smooth surface by ECMP, the conditions under which the polishing rate is higher than the oxidation rate are necessary.

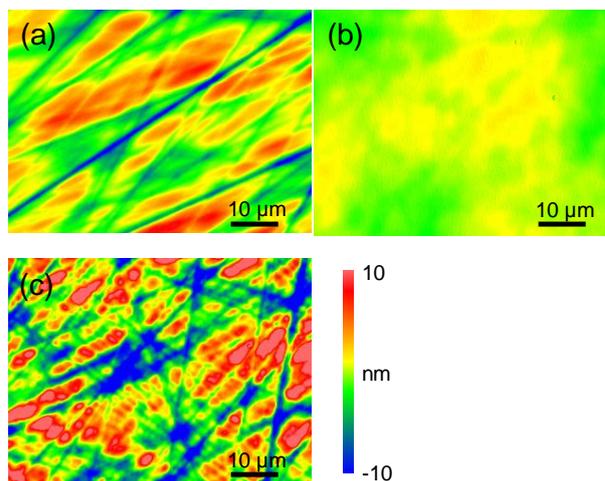


Figure 3. SWLI images of polished SiC surfaces. (a) Diamond abrasive lapped surface (p-v: 24 nm, rms: 3.2 nm), (b) ECMP processed surface with rotation speeds of 70 rpm (Pad) and 150 rpm (Wafer) (p-v: 7.4 nm, rms: 0.85 nm), (c) ECMP processed surface with rotation speeds of 30 rpm (Pad) and 45 rpm (Wafer) (p-v: 46 nm, rms: 5.8 nm).

4. Conclusions

The relationship between the balance of the oxidation rate and the removal rate in ECMP and the surface morphology after polishing was experimentally investigated. With a high relative speed of the polishing pad and SiC wafer, the polishing rate was higher than the oxidation rate and a flat surface without residual oxide layer was obtained. In contrast, with a low relative speed of the polishing pad and SiC wafer, an oxide layer remained on the polished surface and many scratches were introduced.

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