

## **Nanoimprint Lithography technology for high volume manufacturing**

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### **Abstract**

Nanoimprint lithography (NIL) has developed from an emerging nano replication technology into a matured and industrially viable manufacturing technology. Since its invention in the mid 90s, it is now by far the fastest and most cost-efficient nano-replication method available on the market. One of the first industrial adaptations of nanoimprint lithography in manufacturing is to enhance light output of LED's [1, 2] and it has been shown that the technology can be used for manufacturing with a high throughput and yield [3] but there are also many other applications with promise such as organic electronics [4] and magnetic media [5]. Obducat uses a IPS®/STU® manufacturing process where no hard materials touch each other during process sequence, see figure 1 (left). The IPS® material is flexible which allows the stamp to adjust to the curvature and roughness of the substrate, thereby giving a uniform residual layer on full wafer scale. This enables imprinting of several different types of wafers such as III/V based wafers, flexible substrates, silicon substrates as well as lenses with a curved surface. Focusing on LED production, the wafers used are typically III/V semiconductor materials grown with epitaxial processes. These types of substrates suffer from growth defects like hexagonal spikes, v-pits, waferbowing, atomic steps and surface corrugations on a scale of few 10µm or even large islands of irregularities. The mentioned irregularities are particularly disturbing when NIL based processes are utilized to create patterns onto the wafer surface. The defects can have a height of several µm, which can cause large areas without nano-patterns, substrate breakage or as in the case where the stamp is applied directly onto the substrate, breakage of the stamp itself. Using the IPS®/STU® manufacturing process easily copes with this since no hard materials touch each other during the entire process sequence. Indeed, this is essential for high volume manufacturing where the imprinted nanostructures must have a consistent quality. This paper will show that

NIL is the preferred technology to produce nanopatterns on GaN substrates used for producing LEDs. In addition, examples of other application areas such as organic electronics will also be shown.

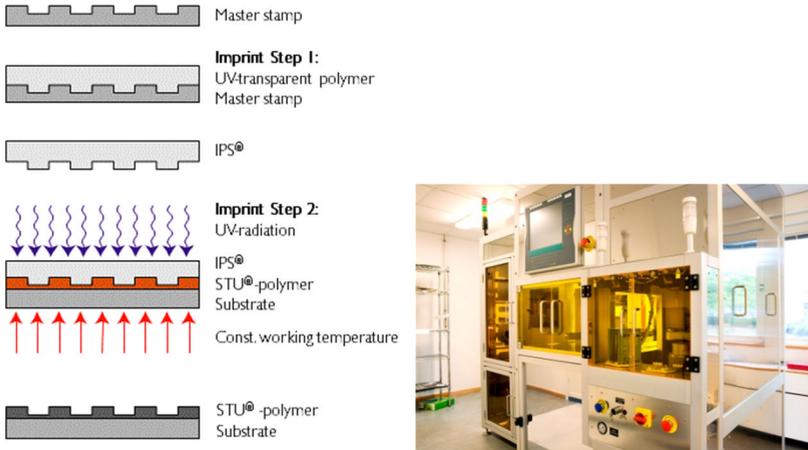


Figure 1: The IPS®/STU® process (left) and the Sindre® 400 (right).

## 1 Experimental

In order to verify that NIL could be used for high volume manufacturing of LED components, a manufacturing run of a series of 8000 imprints was performed. The results have been reported in full previously [3]. The nickel stamp used had recess photonic-crystal-like dot patterns on a 2-in. area with holes measured to a depth of 157 nm, a pitch of 451 nm and a dot width of 234 nm. Two-inch sapphire substrates with GaN and a SiO<sub>2</sub> layers on top were used in the STU\_ process. The substrates were spin-coated with TU2 resist. Every 50th substrate imprint between 2050th and 3450th and between 3525th and 4025th as well as number 8000th were measured in five positions using a Veeco Dimension 3100 Atomic Force Microscope. The measurement points were located in the center and at the edges. At each point, feature pitch, depth and residual layer thickness were measured. The results can be seen in figure 2 that show the pitch as a function of number of imprints. The figure show that the replicated nanostructures lies very close to the pattern on the stamp.

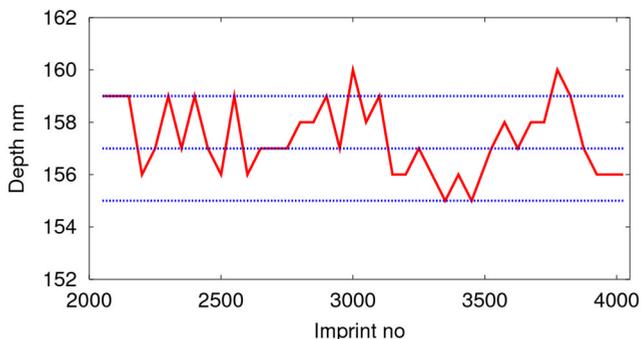


Figure 2: The depth as a function of the number of imprint.

In addition, NIL and in particular the IPS®/STU® process can also be used with flexible substrates. Flexible substrates are of particular interest in organic electronics applications where they can be used to create very cheap electronics. Perhaps the most simple building block in electronics is the transistor. A typical organic transistor consists of source, drain, gate, dielectric and semiconductor. In particular, the channel length (length from source to drain) should be as small as possible. Therefore the width of the gate finger is a very important part, as well as the distance between drain and source. Another contributing factor is the thickness of the dielectric layer. Figure 3 and 4 show examples of a bottom gate feature produced with NIL using a so called lift-off process to deposit a metal pattern on a polymer film.

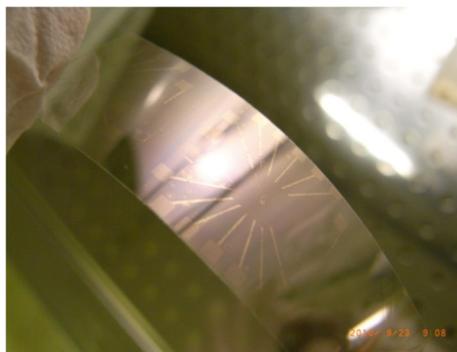


Figure 3: Gold micro and nanopatterns produced on a polymer sheet.

In this case, two layers of resist was spin coated on the PC substrates. A lift off resist (LOR from Microchem) followed by TU2 from Obducat. The stack was imprinted in an Eitre 8” nanoimprint lithography tool using the IPS®/STU® process. The thin residual layer was removed using a short oxygen plasma process. Au was evaporated on the nano-patterns using a Cryofox thin film deposition plant from Polyteknik. Finally, the lift off process was finalized by removing the lift off resist by a quick submersion in MF 322 (TMAH – tetramethyl ammonium hydroxide). The solvent efficiently removed the lift off resist without causing any damage to the PC film. This process has been shown to work to replicate line features of 23 nm.

## 2 Conclusion

It has been shown that NIL is an industry process that can produce nanopatterns on various substrates for different applications.

## 3 Acknowledgements

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## References:

- [1] Kim S H, Lee K-D, Kim J-Y, Kwon M-K, Park S-J, *Nanotechnology* **18**, 2007
- [2] Huang H W, Lin C H, Yu C C, Lee B D, Chiu C H, Lai C F, Kuo H C, Leung K M, Lu T C, Wang S C, *Nanotechnology* **19**, 2008
- [3] Eriksson T, Yamada S, Krishnan P V, Ramasamy S, Heidari B, High volume nanoimprint lithography on III/V substrates: Imprint fidelity and stamp lifetime, *Microelectronic Engineering*, Vol 88, Issue 3, Pg 293 – 299, 2011
- [4] Löfstrand A., Rindzevicius T., Ring J., Eriksson T., Heidari B, High Volume Nanoimprint Lithography: application area organic electronics, Proceedings of the 4M conference, Stuttgart, 2011
- [5] Brombacker C., Grobis M., Lee J. Fidler J. Eriksson T. Werner T., Hellwig O., Albrecht M., L1<sub>0</sub> FePtCu bit patterned media, *Nanotechnology* 23, 2012