# 2D and 3D Interconnect Fabrication by Picosecond Laser Induced Forward Transfer

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## Abstract

Interconnects are an important cost driver in advanced 3D chip packaging. This holds for Through Silicon Vias (TSV) for chip stacking, but also for other integrated Si-technology. Especially in applications with a low number (<100 mm$^{-2}$) of relatively large (10-20 µm diameter), high aspect ratio (1:5-1:20) vertical interconnects (TSVs), conventional wafer level plating processes are slow and become cumbersome with increasing aspect ratio, thus becoming cost ineffective. Hence, industrially feasible alternative deposition processes are of interest for advanced interconnects.

LIFT is a maskless direct-write process with industrial potential. It is a single step, dry process under atmospheric (clean room) conditions. It is suitable for different types of interconnect fabrication, without the need for wet chemicals or high temperatures. The paper reports on the investigations towards minimum feature size, morphology and resistivity of 2D and 3D copper structures built using picosecond LIFT. It will be shown that very promising structures could be realized. Possible applications for micro electronics manufacturing are discussed.

## 1 LIFT as a manufacturing process

Laser induced deposition processes have been investigated widely, as extensively described in a review by Banks [1]. Many varieties of the LIFT process exist [1,2,3]. However, as yet no attempts have been made to apply the LIFT process in an industrial setting. The purpose of our research is to investigate and consequently develop the industrialization of the LIFT process to create micron-sized electrical interconnects. Therefore we started with the investigation of feature size and electrical resistivity of the deposited material.

A pure metal donor on a transparent carrier as well as ultra-short picosecond (ps) laser pulses were selected for the experiments (Figure 1). The downward facing donor layer is positioned close to the substrate surface. The thickness of the resulting air-gap between donor and substrate is typically 10-50 µm.

In this way, metal deposits in the µm range can be formed using a ps-laser with a spot size of 5-20 µm focused onto the metal layer. To build 2D and 3D structures, overlapping droplets need to be deposited (Figure 1), while scanning the substrate ($v_{substrate}$). The donor layer is fully used for each laser shot. Hence the donor layer needs to be refreshed at a higher rate ($v_{donor}$) than the scanning motion.

## 2 Experimental results

Using a straightforward laboratory-scale donor refreshment set-up, experiments have been performed in green and UV light using the picosecond laser machining facility at the University of Twente.

### 2.1 2D feature size and line conductivity

First the deposited feature size was investigated as a function of laser power and air gap distance. A typical result of this study is shown in Figure 2-a. It can be seen that single droplets with dimensions ≤ 5 µm are formed (indicated by orange box). At higher laser power, splashes with dimensions in the 5-10 µm range are formed. The latter setting was chosen to generate conductive lines (Figure 2-b).

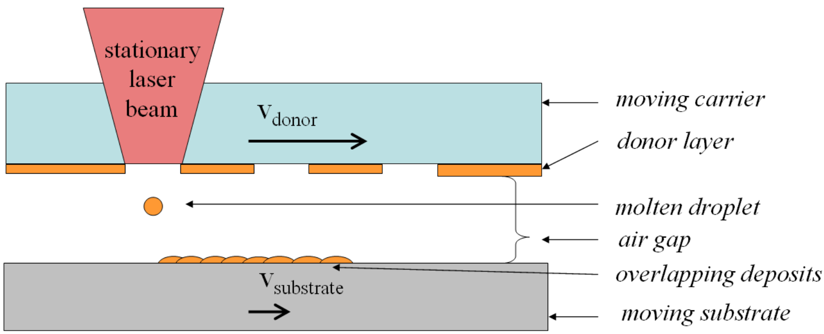
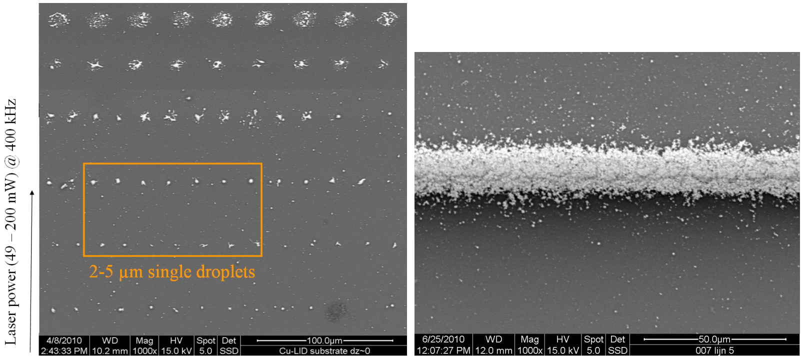


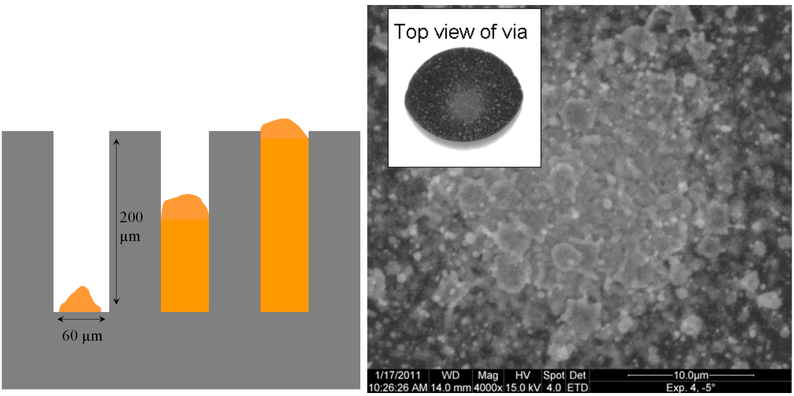

Figure 1 : Schematic overview of the LIFT process. To achieve overlapping deposits, the donor has to be refreshed. As a result the donor moves faster ($v_{donor}$) than the substrate ($v_{substrate}$) with respect to stationary the laser beam.

The conductivity of this line was measured to be 5.8 times the electrical bulk resistance of copper using a 4-point resistance measurement. Such a resistivity is comparable to other direct-write technologies and is amply sufficient to generate functional interconnecting structures [4].




a b

Figure 2 : SEM images of a) a matrix of copper deposits fabricated using an air gap of several µm. The process window that shows droplets/deposits in the range 2-10 µm is indicated (orange rectangle). b) a line (cross section: 3x15µm) produced by 15 overlapping deposits.




a b

Figure 3 : Deposition inside a high AR TSV a) Schematic overview with the dimensions of the via. b) SEM image of the deposited copper droplets on the bottom of the via.

### 2.2 3D feasibility

The same settings as in Figure 2 were also applied to deposit droplets inside a high AR TSV (Figure 3).Based upon visual analysis of the SEM pictures it seems likely that the droplets reached the bottom in a molten state, given the splash shaped deposits. Also, the deposition accuracy is maintained over this larger distance i.e. the majority of the droplets landed within a diameter of about 20 µm. Hence, filling high AR structures with copper using LIFT appears to be a feasible approach. Vias with a smaller diameter will be used to study the complete filling of the vias.

## 3 Conclusions on Industrial feasibility of LIFT

Production speed of LIFT can be estimated by extrapolating the current results based on properties of state-of-the-art picosecond lasers. This is presented in Table 1. It can be seen that, for different types of applications, production speeds can be achieved that justify further research. Topics like: wetting, adhesion and porosity still need attention. Furthermore, a high throughput industrial production tool must be designed.

Manufacturing feasibility of LIFT has not been published before on this scale. Hence, the results currently achieved are a unique first step towards industrial application of LIFT as a micro-manufacturing technology.

Table 1: Estimates of industrial production speeds, assuming state-of-the-art picosecond laser parameters: 2MHz repetition rate, single beam and 10 µm deposit size. A deposit overlap percentage is assumed (% overlap), as well as an effective laser repetition rate based on a first estimate of substrate and donor positioning.

| | **TSVs** | **Conductor lines (solar)** | **Printed wire bonds** |
|---|---|---|---|
| Overlap | *100 deposits/via* | *90%* | *90%* |
| Laser rep. rate | *1 MHz* | *1.6 MHz* | *200 kHz* |
| Feature size | *10x50 µm* | *10µm line width* | *3µm x 10µm x 3mm* |
| Process speed | *5-50 wafers/h* | *1.6 m/s* | *133 wires/s* |

**References:**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