FPGA Based Control System for Coupled Highly Dynamic Axes in Ultra-Precision Machining

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Abstract

The requirements for the dynamics of mechatronic axis systems used in production machines for high-end applications increase steadily. Additionally, in ultra-precision machining a high positioning accuracy is requested. One application example of highly dynamic axes is the manufacturing of non-rotationally symmetric optical components in a turning process. These optics or molding tools are manufactured by diamond machining to achieve a very low surface roughness. In the turning process the non-rotationally symmetric part of the work piece geometry requires a highly dynamic movement of the cutting tool. Especially structured geometries need very high frequencies for an economical process. The applied highly dynamic axes, either if integrated into the machine system or used as auxiliary axes, usually cannot be controlled with standard servo control systems. Especially piezo-based mechatronic systems require high bandwidth feedback control loops.

1 FPGA based Servo Control System

The basic platform for the servo control system presented in this paper is a hybrid system, consisting of a microprocessor-based high level part for setpoint processing and an FPGA-based (Field Programmable Gate Array) low level part. In a microprocessor system the digital hardware structure is fixed. Additionally, the sensors and actors of the control system cannot be connected to the arithmetical unit directly, but over a peripheral bus system. This implies a significantly high input/output latency time dominating the dynamic performance of the control loops. Compared to a microprocessor, the digital hardware structure of a computation system, which can be implemented within an FPGA, is freely programmable and reconfigurable and can be adapted to the application. Especially critical paths in the digital algorithms can be optimized. While programs on a microprocessor based system are as a matter of principle sequentially processed, on an FPGA based system algorithms can be designed in parallel which is especially effective for high bandwidth control loops. With these techniques the overall latency of the control algorithms can be optimized to a minimum. Compared to standard servo control systems, due to the low latency, the presented approach does not constrain the dynamic performance of the feedback control system consisting furthermore of power electronics, mechanics and sensors.

2 Axes and Control Loops

Fig. 1 shows the information flow of the fundamental control signals between the FPGA based servo control system and the electro-mechanical axes containing sensors and actors. The position control loop for the Fast Tool is closed over a voltage controlled output stage for the piezo actuator and a capacitive position sensor with processing electronics. The stroke of the system due to the mechanics and the range of the capacitance probe is limited to maximally 35 µm. The transfer behavior of the electro-mechanical system is limited to 2 kHz due to mechanical eigenfrequencies. The sample rate is required to be at least 20 kHz, a factor of 10 higher than the bandwidth, using the common rule of thumb regarding minimum demands on sampling controls. To utilize the full bandwidth of the mechanics, the actual control clock with 250 kHz is implemented higher, though, to provide a phase decay which is as low as possible in the range of higher frequencies. This phase decay is critical for the performance of the transfer behavior of the axis.

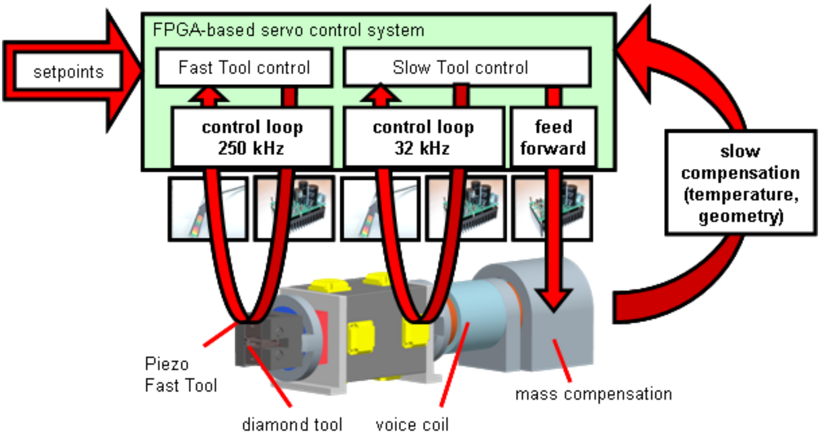

Fig. 1: Information flow and control loops of the FPGA-based servo control system

The same requirements for the sampling control on a smaller scale apply for axes with lower dynamics, too. The mechanical system supporting the piezo-based Fast Tool consists of a long stroke voice coil driven, hydrostatically supported axis called Slow Tool. This system features an electro-mechanical bandwidth of around 100 Hz and a maximum stroke of 25 mm. The Slow Tool system also benefits from the high control clock, but essentially profits from the interpolator for the sin/cos encoded linear scale position sensor implemented in the FPGA. Compared to standard interpolator circuits, which only feature input bandwidths of around 500 kHz as a maximum, the interpolator implemented into the FPGA reaches more than 2 MHz. The important consequence of this input bandwidth is the impact onto the velocity limits, which limit the operation area of the axis. Assuming a linear scale division of 250 nm used in the Slow Tool, the velocity limit can be extended from 0.125 mm/s to more than 0.5 mm/s. Furthermore, the servo control system supports the feed forward control of an optional mass compensation unit, enabling decoupling strategies with the required low latency.

3 Control Loop Performance

The control loops benefit significantly from the achievable control clocks using the FPGA-based control system. Fig. 2 shows measurements of the step response on 2 µm and the small signal transmission behavior of the Fast Tool system using two different control platforms with a standard PI controller for comparability. The reference system with an architecture based on a microprocessor (Processor in Fig. 2) features a sample rate of 40 kHz. The FPGA control loop is clocked with 250 kHz. In the time domain the response time decreases from 400 µs to 300 µs, where a

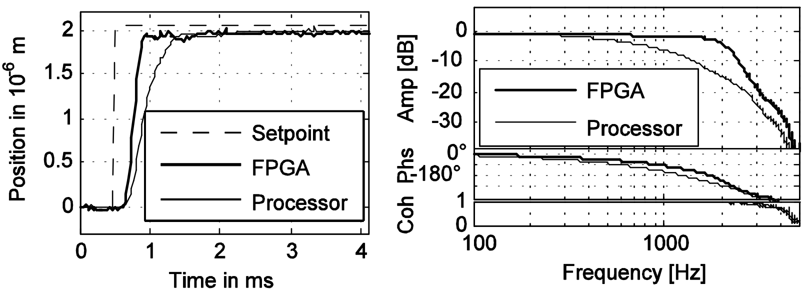

Fig. 2: Comparison of FPGA and microprocessor frequency and step response

significant amount of around 200 µs arises from the time response of the applied piezo amplifier, which is clocked with 100 kHz, and the signal processing of the capacitance sensor. As shown in Fig. 2, the bandwidth specified by the edge frequency of the phase at –90° is increased from around 600 Hz to 900 Hz, with a gain in phase achieved of 40° at 900 Hz. The bandwidth regarding the –3 dB criterion is even more improved from around 600 Hz to 2 kHz.

4 Evaluation of Using FPGAs in Controlling Highly Dynamic Axes

However, while it is technically possible, FPGAs are not well suited for the implementation of mathematically complex algorithms, in contrast to microprocessors with highly clocked digital logic which is exceedingly optimized for these tasks. The implied performance discrepancy particularly applies for algorithms using floating point arithmetic. For reasons of structure complexity yet applicable in the used Xilinx Virtex 4 FPGA only Single Precision Floating Point (IEEE754) is used, while Double Precision Floating Point is common in modern microprocessors. For feedback control loops, nevertheless, the advantages of the FPGA based control platform regarding the achievable extremely low latency, heavily outweigh the disadvantages regarding computing power, as can be seen in the measurement results presented in the paper.

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